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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,678	09/29/2003	Yasushi Aoki	8022-1060	8269

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,678	AOKI, YASUSHI	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *29 September 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 9 is rejected under 35 U.S.C. 102(e) as being anticipated by Feldman (US 6,781,445).

Feldman discloses in Fig. 4 an integrated circuit comprising a logic circuit developing first and second sinusoidal signals (VIN+, VIN-) whose phases are different by 180 degrees; and a differential output circuit (420, 430, 440 - 480) responsive to the first and second sinusoidal signals to develop first and second complementary output signals (VOUT-, VOUT+) on first and second outputs, respectively, wherein the differential output circuit includes an inductive element (480) connected between the first and second outputs.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawashima (US Pat. 5,699,305) in view of Onodera et al. (US Pat. 5,121,284).

With regard to claims 1 and 2, Kawashima discloses in Fig. 7 a differential output circuit comprising a first input (n1) receiving a first input signal; a second input (n2) receiving a second input signal complementary to the first input signal; a first N-channel transistor (72) having a source connected to the first input, a gate receiving a power supply potential (VCC), and a drain connected to the first output (n3); a second N-channel transistor (73) having a source connected to the second input, a gate receiving the power supply potential, and a drain connected to the second output (n4); a first P-channel transistor (66) having a source receiving the power supply potential, a gate connected to the second input, and a drain connected to the first output; and a second P-channel transistor (67) having a source receiving the power supply potential, a gate connected to the first input, and a drain connected to the second output. Fig. 7 of Kawashima shows a circuit meeting all of the claimed limitations except for a resistor element (31 in instant Fig.2) connected between the first and second outputs. Onodera et al. teaches in Fig. 3 a circuit having a load (20), which comprises a resistor element (RL) and an inductor element (L) connected between the first and second outputs (35, 37) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement the load taught by Onodera et al. in the circuit of the prior art in order to provide a desired output impedance to drive a subsequent circuit. Furthermore, the transistors in Kawashima's circuit are MOSFETs instead of MISFETs as recited in the claim. However, it will be understood that the MOSFETs of Kawashima can be practiced with other types of transistors as well, including MISFETs (see column 1, line 28 through column 2, line 31 of Sato et al. US

Pat. 4,984,201). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to use the transistors of the prior art with MISFETs, instead of MOSFETs, in order to meet the specific condition of the particular application.

With regard to claim 5, Kawashima discloses in Fig. 7 a differential output circuit comprising a first input (n1) receiving a first input signal; a second input (n2) receiving a second input signal complementary to the first input signal; an output circuit (66, 67,72, 73) developing first and second complementary output signals on first and second outputs (n3, n4) in response to the first and second input signals, respectively. Furthermore, the limitation "an inductive element connected between the first and second outputs" is also met by the references; note the above discussion with regard to claims 1 and 2.

With regard to claim 7, Kawashima discloses in Fig. 7 a circuit comprising a logic circuit (74,75) developing first and second clock signals complementary to each other (at nodes **n1** & **n2** when the input signals **in** and **/in** alternate at a certain frequency); and a differential output circuit (66, 67,72, 73) responsive to the first and second clock signals to develop first and second complementary output signals on first and second outputs (n3, n4), respectively. Furthermore, the limitation "wherein the differential output circuit includes an inductive element connected between the first and second outputs" is also met by the references; note the above discussion with regard to claims 1 and 2.

With regard to claims 6 and 8; note the above discussion with regard to claims 1 and 2.

5. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawashima in view of Onodera et al., as applied to claims 1-2 above, and further in view of Liewellyn (US Pat. 6,724,248).

The above discussed the differential output circuit of the prior arts meet all of the claimed limitations except for the limitation that the load circuit (31-33 and 34-36 in instant Figs. 5-6) comprise inductors and resistors connected in series between the first and second outputs, as recited in the claims. Liewellyn teaches in Figs. 1-3 a circuit having a load (180), which may be inductive, capacitive, resistive, or any combination thereof. Thus, it would have been obvious to one skilled in the art at the time of applicant's invention was made to incorporate any combination of inductive, capacitive, resistive in any configuration which is in each case optimally matched to its application.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Feldman.

With regard to claim 10, the differential output circuit further includes first and second inputs receiving the first and second sinusoidal signals, respectively, a first N-channel transistor (440) having a source connected to the first input, a gate receiving a power supply potential (see column 5, lines 63-64), and a drain connected to the first output, a second N-channel MISFET (450), a first P-channel transistor (460), and a second P-channel transistor (470). The above discussed circuit of Feldman meets all of the claimed limitations except for the limitation that the transistors are MISFETs instead of MOSFETs. However, it will be understood that the MOSFETs of Kawashima can be practiced with other types of transistors as well, including MISFETs (see column 1, line 28 through column 2, line 31 of Sato et al. US Pat. 4,984,201). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to use the transistors of the prior art with MISFETs, instead of MOSFETs, in order to meet the specific condition of the particular application.

7. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawashima in view of Onodera et al., and further in view of Fukui (US Pat. 6,114,906).

In view the discussion with regard to claims 1 and 2 above, the circuit of the references meets all of the claimed limitations except that the logic circuit of the reference (74 & 75 in Fig. 7 of Kawashima) are pull-down transistors instead of pull-up N-channel transistors as recited in the claims. Fukui teaches in Fig. 4 a logic circuit being configured in a differential output circuit and having pull-up N-channel transistors (204, 205) used for pull-up input signals. Therefore, it would have been obvious to one of ordinary skill in the art to replace the pull-down transistors in the logic circuit of Kawashima with the pull-up N-channel transistors taught by Fukui in order to meet the specific input levels of the particular application. It has been held that discovering an optimum range or to optimally match to an application is obvious to the skilled artisan. See *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Bosnyak et al. (US 5,767,699) is cited as of interest because it discloses a fully complementary differential output driver for high speed digital communications circuit.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN
October 6, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800